REMARKS

Claims 1-3 and 17-21 are pending in the application. Claims 1, 17 and 18 are rejected under 35 U.S.C. §102(e). Claims 2, 3, 19 and 20 are rejected under 35 U.S.C. §103(a). Claim 21 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw all outstanding rejections.

I. PREMATURE FINAL REJECTION:

The Examiner has withdrawn the finality of the previous office action (mailed on September 13, 2004) in view of Applicants' 1.116 Reply (mailed on October 5, 2004). Paper No. 17, page 2. However, the Examiner has made the current office action (Paper No. 17) final allegedly because Applicants proposed amendments in Applicants' 1.116 Reply (mailed on October 5, 2004). There were no proposed amendments in Applicants' 1.116 Reply (mailed on October 5, 2004). An Examiner cannot make an office action final where the Examiner introduces a new ground of rejection, as in the present office action, that was neither necessitated by Applicants' amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 C.F.R. §1.97(c) with the fee set forth in 37 C.F.R. §1.17(p). M.P.E.P. §706.07(a). Since Applicants did not propose any amendments in Applicants' 1.116 Reply and since no information disclosure statement was filed during the period set forth in 37 C.F.R. §1.97(c), the Examiner's finality is premature. Applicants respectfully request the Examiner to withdraw the finality of the present office action.

II. REJECTIONS UNDER 35 U.S.C. § 102(e):

The Office Action has rejected claims 1, 17 and 18 under 35 U.S.C. §102(e) as being anticipated by Lee et al. (U.S. Patent No. 6,197,639) (hereinafter "Lee"). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. § 2131.

Applicants respectfully assert that Lee does not disclose "at least one component including a polysilicon layer having a top surface, wherein the at least one component is formed on a field oxide region configured to separate the plurality of gate stacks" as recited in claim 1. The Examiner cites elements 57, 63 of Lee as disclosing an at least one component. Paper No. 17, page 2. The Examiner further cites element 53 of Lee as disclosing a field oxide region. Paper No. 17, page 2. Applicants respectfully traverse the assertion that Lee discloses the above-cited claim limitation.

Lee instead discloses that a field oxide layer 53 is formed on a silicon substrate 51 to define an active region. Column 3, lines 40-41. Lee further discloses that a tunnel oxide layer 55 is formed on the silicon substrate 51 having the field oxide layer 53 and the active region, to a thickness of 100Å. Column 3, lines 41-44. Lee further discloses that a first polysilicon layer 57 for forming a floating gate is formed on the tunnel oxide layer 55. Column 3, lines 44-45. Lee further discloses that after forming a gate oxide layer 61 in the periphery region, a second polysilicon layer 63 and a tungsten silicide layer 65, as a control gate, are formed in the cell array region and the periphery region. Column 3, line 65 – column 4, line 1. As illustrated in Figure 6, second polysilicon layer 63 is formed on ONO layer 58. There is no language in Lee that discloses that polysilicon layers 57, 63 are a component. Neither is there any language in Lee that discloses that polysilicon layers 57, 63 are formed on a field oxide region. Thus, Lee does not disclose all of the limitations of claim 1, and thus Lee does not anticipate claim 1. M.P.E.P. §2131.

Applicants further assert that Lee does not disclose "a silicide on the top surface of the polysilicon layer of the at least one component", as recited in claim 1, for at least the reasons stated above.

Applicants further assert that Lee does not disclose "an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the

insulating layer having a plurality of contact holes therein", as recited in claim 1, for at least the reasons stated above.

Applicants further assert that Lee does not disclose "a component located on said field oxide region, wherein said component is formed from one of said first and said second polysilicon layer" as recited in claim 17. The Examiner cites elements 57, 63 of Lee as disclosing a component. Paper No. 3, page 3. Applicants respectfully traverse the assertion that Lee discloses the above-cited claim limitation.

Lee instead discloses that a gate stack that includes both the first and second polysilicon layers (elements 57 and 63) is formed on field oxide layer 53 as illustrated in Figure 7. Claim 17 recites both a gate stack and a component. Under the rule of claim differentiation, a gate stack may not be interpreted as a component. Furthermore, the gate stack is not formed from one of the first and second polysilicon layers, as required by claim 17, but from both of the first and second polysilicon layers. Thus, Lee does not disclose all of the limitations of claim 17, and thus Lee does not anticipate claim 17. M.P.E.P. §2131.

Applicants further assert that Lee does not disclose "a silicide layer formed on said component", as recited in claim 18, for at least the reasons stated above.

Claim 18 recites combinations of features including the combinations of claim 17, and thus is not anticipated for at least the reasons claim 17 is allowable.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Lee, and thus claims 1, 17 and 18 are not anticipated by Lee.

III. REJECTIONS UNDER 35 U.S.C. § 103(a):

The Examiner has rejected claims 2, 3, 19 and 20 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Ma et al. (U.S. Patent No. 5,939,753) (hereinafter "Ma"). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw these rejections.

A. The Examiner has not presented a source of motivation for modifying Lee with Ma.

The Examiner states that the motivation to modify Lee with Ma to have a silicide layer formed on a component include either titanium silicide or cobalt silicide, as recited in claims 2-3 and 19-20, is because "such materials are equivalence for their use in the semiconductor art as to form a dual-layer structure with low resistance, which is made up of a polysilicon and metal silicide." Paper No. 17, page 5. The motivation to modify Lee with Ma must come from one of three possible sources: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner has not provided any evidence that his motivation comes from any of these sources. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 2, 3, 19 and 20. *Id.*

B. By modifying Lee with Ma, the principle of operation of Lee would change.

If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 370 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). For the reasons discussed below, Applicants submit that by modifying Lee with Ma, the principle of operation in Lee would change and subsequently render the operation of Lee to perform its purpose unsatisfactorily.

Lee teaches a floating gate formed of the first polysilicon layer pattern 57a, a dielectric layer pattern 58a, a control gate including a silicide layer pattern 65a and a

second polysilicide layer 63a, an anti-reflective layer pattern 67a and a nitride layer pattern 69a are formed, thereby completing a stack gate in the cell array region of the silicon substrate 51. Column 4, lines 18-24. As illustrated in Figure 6, the silicide layer pattern 65a covers the entire second polysilicide layer 63a. Lee further teaches that over-etching occurs because the step difference in the cell array region is larger than the step difference in the periphery region. Column 1, lines 61-63. Lee further teaches fabricating a NOR flash memory device, capable of reducing etching damage, which also simplifies a process for forming a contact region of a cell array region and a periphery region. Column 1, line 67 – column 2, line 3.

Ma, on the other hand, teaches titanium silicide regions that cover portions of polysilicon resistor 58 as illustrated in Figure 7. Column 7, lines 48-51.

By combining Lee with Ma, Lee would no longer be able to reduce etching damage as the silicide layer pattern 65a would no longer cover the entire second polysilicide layer 63a. As stated above, Ma teaches that the silicide covers portions of a polysilicon resistor. Hence, by combining Lee with Ma, the silicide layer 65a in Lee would no longer cover the entire polysilicide layer 63a but only portions of the second polysilicide layer 63a. By modifying Lee so that the silicide layer 65a covers portions of the second polysilicide layer 63a, Lee would not be able to reduce etching damage, which is the principle of operation of Lee. Thus, by modifying Lee with Ma, the principle of operation in Lee would change, and subsequently render the operation of Lee to perform its purpose unsatisfactorily. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2, 3, 19 and 20. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

C. The Examiner has not presented any objective evidence for modifying Lee with Ma.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to

make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id*

As stated above, the Examiner's motivation for modifying Lee with Ma to have a silicide layer formed on a component include either titanium silicide or cobalt silicide, as recited in claims 2-3 and 19-20, is because "such materials are equivalence for their use in the semiconductor art as to form a dual-layer structure with low resistance, which is made up of a polysilicon and metal silicide." Paper No. 17, page 5. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation does not address as to why one of ordinary skill in the art with the primary reference (Lee) in front of him would have been motivated to modify Lee with the teachings of the secondary reference (Ma). Lee teaches a control gate that includes a silicide layer pattern 65a that covers the entire second polysilicide layer 63a. Column 4, lines 20-21 and Figure 6. As stated above, Ma teaches titanium silicide regions that cover portions of polysilicon resistor 58 as illustrated in Figure 7. Column 7, lines 48-51. Stating that titanium silicide or cobalt silicide are equivalent materials does not address as to why one of ordinary skill in the art would modify Lee with Ma such that the silicide layer (silicide layer pattern 65a), as taught in Lee, which may include titanium or cobalt silicide, would cover a portion and not the entire polysilicide layer 63a since Ma teaches silicide regions that cover portions of polysilicon resistor 58. The Examiner must provide a suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art to modify the silicide layer (silicide layer pattern 65a), as taught in Lee, which may include titanium or cobalt silicide, to cover only a portion and not the entire polysilicide layer 63a. M.P.E.P. §2143. As the Examiner has not provided such motivation, but instead relies upon his own subjective opinion, the Examiner has not

presented a *prima facie* case of obviousness in rejecting claims 2, 3, 19 and 20. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002); M.P.E.P. §2143.

D. The Examiner has not presented a reasonable expectation of success when combining Lee with Ma.

The Examiner must present a reasonable expectation of success in combining Lee with Ma in order to establish a *prima facie* case of obviousness. M.P.E.P. §2143.02.

Lee teaches fabricating a NOR flash memory device, capable of reducing etching damage, which also simplifies a process for forming a contact region of a cell array region and a periphery region. Column 1, line 67 – column 2, line 3. Ma, on the other hand, teaches a monolithic integrated circuit and a process for fabricating the monolithic integrated circuit that performs both radio frequency analog circuit and digital circuit functions. Column 1, line 65 – column 2, line 27. The Examiner has not presented any evidence that there would be a reasonable expectation of success in combining Lee, that relates to a NOR flash memory device with reduced etching damage, with Ma, that relates to a monolithic integrated circuit that performs both radio frequency analog circuit and digital circuit functions. The Examiner must provide objective evidence as to how a NOR flash memory device with reduced etching damage would be combined with a monolithic integrated circuit that performs both radio frequency analog circuit and digital circuit functions. M.P.E.P. §2143.02. Since the Examiner has not provided such evidence, the Examiner has not presented a reasonable expectation of success in combining Lee with Ma. M.P.E.P. §2143.02. Accordingly, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 2, 3, 19 and 20. M.P.E.P. §2143.02.

IV. ALLOWABLE SUBJECT MATTER:

The Examiner has objected to claim 21 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim any intervening claims. Paper No. 17, page 5. Applicants thank the Examiner for the indication of allowability of claim 21.

V. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 1-3 and 17-21 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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